First Hit Fwd Refs

End of Result Set

Generate Collection Print

L7: Entry 9 of 9 File: USPT Sep 15, 1992

DOCUMENT-IDENTIFIER: US 5148545 A
TITLE: Bus device which performs protocol confidential transactions

Abstract Text (1):
A bus device of a first type uses a first arbitration protocol. The first-type device is designed for use in a computer system having a communications bus, and one or more other bus devices connected to the bus, including possible first-type bus devices which also use the first arbitration protocol and one or more second-type bus devices which use a second, different, arbitration protocol. The first-type bus device includes a protocol specific memory for storing information; means for monitoring the bus to determine whether the current bus master of the bus arbitrated in the manner of the first or second arbitration protocols; and means for denying the current bus master the ability to access information stored in the protocol specific memory if the means for monitoring determines the bus master arbitrated according to the second arbitration protocol.

Detailed Description Text (64):
In general, the assertion of ACK during the first data cycle indicates correct receipt of Command/Address information, together with the ability of the Slave to take the requested action, i.e., return read data. Conversely, the assertion of NO ACK indicates either an error in transmission of the command or some other inability of a Slave to respond. The assertion of STALL allows the Slave to extend the transaction in order to prepare itself to provide the read data requested by the Master, while the assertion of RETRY indicates current inability to respond to the command, accompanied by a request that the Master try again at a subsequent time. RETRY is appropriately used when the expected response time of the Slave would be so long that it would be inefficient to extend the transaction an excessive number of cycles by asserting general STALL responses.

Detailed Description Text (323):
The Imbedded Arbitration cycle of the DMA's second WRITE is identical to that contained in its first WRITE, except that the COM chip responds to the second post-data ACK signal received from the Slave in response to the first WRITE, and except that the node deasserts the DMA.sub.-- REQUEST signal during this cycle. This deassertion of the DMA.sub.-- REQUEST signal indicates that the DMA transaction is to end with the current, in this case, second, individual WRITE transaction. It should be noted, however, that the node could be programmed to delay this deassertion of the DMA.sub.-- REQUEST signal, up until approximately 150 nanoseconds into the last data cycle in the last desired individual WRITE transaction. The chip monitors the DMA.sub.-- REQUEST line, and it will not start another individual transaction if that line is deasserted before approximately 150 nanoseconds into the last data cycle. If DMA.sub.-- REQUEST is not deasserted by this time, the chip will not have time to prevent another transaction from starting on the next cycle, and thus, it will perform at least one more complete individual transaction. Thus it can be seen that the DMA.sub.-- REQUEST line performs a dual function. It informs the chip when to seek to start, and when to end, DMA transactions.

CLAIMS:

3. A bus device of a first type which uses a first arbitration protocol, and which is connected to a communications bus of a computer system, and one or more other bus devices connected to the bus, including zero or more additional first type bus devices which use said first arbitration protocol and one or more bus devices of a second type, which use a second, different, arbitration protocol according to which second-type devices arbitrate in a different manner than said first-type devices, said first-type bus device comprising:

means for arbitrating according to said first arbitration protocol;

protocol specific memory means for storing information;

means for monitoring said bus to determine when one of said other bus devices obtains control of the bus, making it the bus master, and whether said bus master arbitrated in the manner of the first or second arbitration protocol;

means for denying said bus master the ability to access information stored in said protocol specific memory when said means for monitoring determines that said bus master arbitrated according to the manner of said second arbitration protocol.

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